In the Claims:

Please amend claims 6, 8 and 18-19 as indicated below. This listing of claims replaces all prior versions.

1-5. (*Cancelled*)

6. (*Currently Amended*) An MIS type semiconductor device, comprising:

a semiconductor substrate,

a gate electrode formed on ~~the~~ a gate insulating film and formed of gate material, wherein the gate electrode comprises:

a first layer of activated crystalline gate material having a first side oriented towards [[a]] the substrate, ~~and~~ a second side oriented away from the substrate and a grain size, the first layer of activated crystalline gate material having a doping level of 10^{19} ions/cm^3 or higher, and

a second layer of gate material at the second side of the first layer of activated crystalline gate material, the second layer of gate material having a grain size,

wherein the grain size of the first layer of activated crystalline gate material is smaller than the grain size of the second layer of gate material.

7. (*Previously Presented*) A semiconductor device according to claim 6, wherein the first layer of activated crystalline gate material has a doping level of about 10^{20} ions/cm^3 or higher.

8. (*Currently Amended*) An MIS type semiconductor device according to claim 6, wherein ~~the~~ a doping implant in the activated gate material has an abruptness of a doping profile of about 2 nm or more.

9. (*Previously Presented*) A semiconductor device according to claim 6, wherein the second layer of gate material consists of amorphous gate material.

10. (*Previously Presented*) A semiconductor device according to claim 6, wherein the second layer of gate material consists of polycrystalline gate material.

11. (*Previously Presented*) A semiconductor device according to claim 6, wherein the grain size in the second layer is below about 40 nm.

12. (*Original*) A semiconductor device according to claim 6, wherein the first layer is crystalline or very fine-grained, with grains below 5 nm.

13. (*Previously Presented*) A semiconductor device according to claim 6, wherein a gate insulator is provided between the semiconductor substrate and the gate electrode.

14. (*Original*) A semiconductor device according to claim 6, wherein the device is a transistor.

15. (*Cancelled*)

16. (*Cancelled*)

17. (*Previously Presented*) A semiconductor device according to claim 6, wherein the first layer of activated crystalline gate material has a doping level of about 5×10^{20} ions/cm^3 or higher.

18. (*Currently Amended*) An MIS type semiconductor device according to claim 6, wherein ~~the~~ a doping implant in the activated gate material has an abruptness of a doping profile of about 1.5 nm or more.

19. (*Currently Amended*) An MIS type semiconductor device according to claim 6, wherein ~~the~~ a doping implant in the activated gate material has an abruptness of a doping profile of about 1 nm.

20. (*Previously Presented*) A semiconductor device according to claim 6, wherein the grain size in the second layer is below about 30 nm.